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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,763	05/11/2001	Heinrich Meyer	71-01	7120

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EXAMINER	
MUTSCHLER, BRIAN L	

ART UNIT	PAPER NUMBER
1753	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,763	MEYER ET AL.	
	Examiner	Art Unit	
	Brian L. Mutschler	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Comments

1. The objections to the disclosure have been overcome by Applicant's amendment.

2. The objection to the claims has been overcome by Applicant's amendment.

3. The rejection of claims 1-9 under 35 U.S.C. 112, second paragraph, has been overcome by Applicant's amendment to the claims.

4. The rejection of claims 1, 2, and 4-9 under the judicially created doctrine of obviousness-type double patenting over U.S. Pat. No. 6,099,711 has been overcome by the terminal disclaimer filed on November 28, 2003.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over DE 195 45 231 A1, herein referred to as DE '231, an optionally in view of Landau (U.S. Pat. No. 6,261,433). The rejection set forth below uses column and line number references provided by the English language version of DE '231, U.S. Pat. No. 6,099,711, which claims priority from DE '231 and therefore discloses the same invention.

DE '231 discloses a method for electroplating copper on circuit boards comprising the following steps:

a) Coating the surface of the substrate with a full-surface metal layer. In Example 1, DE '231 uses a circuit board having recesses (borings) in its surface that is provided with a thin copper laminate on the surfaces and a thin copper layer in the recesses, i.e., a substrate surface that has been coated (col. 12, lines 8-15).

b) Full surface deposition of copper layers having a uniform layer thickness by an electrolytic metal deposition method. In Example 4, a uniform layer of copper was electroplated on the copper foil covering the circuit board (col. 13, lines 16-21). The copper was deposited using a bath, wherein the deposition step comprised:

   i. A copper ion source, additives to improve the physical-mechanical properties, and a Fe(II) compound (col. 11, line 56 to col. 12, lines 6).

   ii. An electric voltage was applied between the substrate and a dimensionally stable, insoluble counter-electrode (col. 13, lines 1-3 and lines 17-19).

The process of electroplating the copper layer and the buildup of the copper layer "structures" the copper layer.

Regarding claim 2, the current can be changed with a sequence of unipolar or bipolar pulses per unit time (figs. 1 and 2; col. 5, line 30 to col. 6, line 5).

Regarding claims 4 and 5, the anodic current pulse is set to at least the current of the cathodic current pulses and is preferably two to three times as high as the value of the cathodic current pulses (col. 5, lines 46-50).

Regarding claim 6, the additive compound disclosed by DE '231 can include polymeric oxygen-containing compounds (e.g., polyethylene glycol), organic sulphur compounds, thiourea compounds and polymeric phenazonium compounds (col. 8, line 26 to col. 2, line 21).

Regarding claims 7 and 8, the counter-electrode may comprise expanded titanium metal coated with iridium oxide, irradiated with fine particles (col. 16, lines 3-5).

Regarding claim 9, iron compounds are used to maintain the concentration of copper ions in the system by dissolution of copper pieces (col. 14, lines 46-67 and col. 16, lines 6-16).

The method of DE '231 differs from the instant invention because DE '231 does not disclose that the substrate can be a semiconductor substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a semiconductor substrate in place of the circuit board substrate disclosed by DE '231 because semiconductor substrates and circuit board substrates have equivalent properties and one skilled in the art would recognize that the method would be capable of forming a copper layer on either type of substrate. Both semiconductor substrates and circuit board substrates are dielectric materials requiring a conductive layer, or seed layer, on which to plate. Since the actual method of electroplating occurs on the seed layer, one skilled in the art would recognize that the

actual "substrate" is irrelevant, i.e., the "substrate" can be any material, because the effective substrate on which the copper layer is plated is the conductive seed layer. Additionally, the prior art has recognized that electroplating on semiconductors is equivalent to electroplating on semiconductors. For example, Landau teaches, "As a result of these process limitations [i.e., the unsatisfactory results of CVD] electroplating, which had previously been limited to the fabrication of patterns on circuit boards, is just now emerging as a method to fill vias and contacts on semiconductor devices" (col. 2, lines 7-19).

7. Claims 1, 2 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ritzdorf et al. (US 2002/0074233 A1) in view of either Schumacher et al. (U.S. Pat. No. 5,976,341) or DE 43 44 387 A1, herein referred to as DE '387. Since the patent issued to Schumacher et al. claims priority to DE '387, and therefore both references disclose the same invention, the column and line number references made below will be made with respect to the English language document.

Ritzdorf et al. disclose a method for electroplating a semiconductor wafer comprising recessed structures, wherein the method comprises the following steps:

a) Coating the semiconductor substrate surfaces with a base layer. The substrate **400** is coated with a barrier layer **423** and a seed layer **425** (fig. 2D; page 3, par. [0036]-[0037]).

b) Full surface deposition of a copper layer having a uniform layer thickness on the base layer. A uniform layer of copper **440** is deposited on the seed

layer **425** by an electrochemical deposition process (fig. 2E; par. [0038]-[0039]). The electroplating step comprises:

i. A copper deposition bath containing a copper ion source and an additive (par. [0044]).

ii. An electric voltage is applied between the semiconductor substrate and an inert anode, which would be dimensionally stable and insoluble in the deposition bath (par. [0031] and [0047]).

c) Structuring the copper layer. In addition to building up the copper layer **440**, excess materially is subsequently removed (fig. 2F; par. [0039]).

Regarding claim 2, the current may be a forward pulsed current or a forward and reverse current (par. [0047]).

Regarding claim 6, the additive may comprise polyethylene glycol, a polymeric oxygen-containing compound (par. [0044]).

The method of Ritzdorf et al. differs from the instant invention because Ritzdorf et al. do not disclose the following:

a. An Fe(II) compound or Fe(III) compound in the copper deposition bath, as recited in claim 1.

b. Inert metals coated with noble metals or oxides of the noble metals are used as the counter-electrode, as recited in claim 7.

c. Expanded titanium metal coated with iridium oxide and irradiated by means of fine particles is used as the counter-electrode, as recited in claim 8.

d. The concentration of the compounds of the copper ion source in the copper deposition bath is kept constant per unit time by contacting copper parts that are dissolved by reacting with Fe(III) contained in the bath, as recited in claim 9.

Regarding claims 1 and 9, Schumacher et al. disclose a method of electrochemically depositing copper on a circuit board substrate and teach the use of Fe(II) compounds and Fe(III) compounds in the deposition bath to generate copper ions and maintain the copper ion concentration (col. 6, lines 37-40; col. 8, lines 37-49). Because inert anodes are used, iron compounds are provided to generate copper ions using copper parts (col. 8, lines 12-49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Ritzdorf et al. to use iron compounds and copper parts to generate copper ions as taught by Schumacher et al. and DE '387 because the iron compounds and copper parts provide the copper necessary for plating copper when inert anodes are used.

Regarding claims 7 and 8, like Ritzdorf et al., Schumacher et al. disclose the use of insoluble counter-electrodes when electroplating copper (col. 8, lines 12-36). Schumacher et al. further teach that titanium anodes with an iridium oxide coating surface treated to be compacted are sufficiently resistant and have a long lifespan (col. 8, lines 17-20). Expanded metal may also be used to increase the effective surface (col. 8, lines 33-36).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the inert counter-electrode in the method of Ritzdorf et al. to use an expanded titanium metal counter-electrode coated with iridium oxide as taught by Schumacher et al. and DE '387 because such an electrode is sufficiently resistant and has a long lifespan for electroplating copper.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ritzdorf et al. (US 2002/0074233 A1) in view of either Schumacher et al. (U.S. Pat. No. 5,976,341) or DE 43 44 387 A1, as applied above to claims 1, 2 and 6-9, and further in view of Loch (U.S. Pat. No. 4,666,567).

Ritzdorf et al., Schumacher et al. and DE '387 describe a method having all of the limitations recited in claims 1, 2 and 6-9 of the instant application, as explained above in section 7.

The method described by Ritzdorf et al., Schumacher et al. and DE '387 differs from the instant invention because they do not disclose the following:

a. The sequence of bipolar pulses comprises cathodic pulses lasting from 20 milliseconds to 100 milliseconds and anodic pulses lasting from 0.3 milliseconds to 10 milliseconds, as recited in claim 3.

Loch discloses a method for electroplating using bipolar pulsed current, wherein the duration of the cathodic (forward) pulses ranges from about 0.5 microseconds to about 300 seconds and the anodic (reverse) pulses last from about 0.5 microseconds to about 150 seconds (col. 3, lines 40-45). Furthermore, Loch teaches a specific example

comprising a forward pulse of about 30 milliseconds followed by a reverse pulse of about 0.5 milliseconds (col. 7, lines 64-67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method described by Ritzdorf et al., Schumacher et al. and DE '387, to have used pulses lasting within the claimed ranges because Loch teaches that a wide range of pulse lengths can effectively be used and specifically teaches the use of pulse lengths within the claimed range that is efficient for plating.

9. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ritzdorf et al. (US 2002/0074233 A1) in view of either Schumacher et al. (U.S. Pat. No. 5,976,341) or DE 43 44 387 A1, as applied above to claims 1, 2 and 6-9, and further in view of GB 2 214 520 A, herein referred to as GB '520.

Ritzdorf et al., Schumacher et al. and DE '387 describe a method having all of the limitations recited in claims 1, 2 and 6-9 of the instant application, as explained above in section 7.

The method described by Ritzdorf et al., Schumacher et al. and DE '387 differs from the instant invention because they do not disclose the following:

a. The peak current of the anodic pulses is at least the same value as the peak current of the cathodic pulses, as recited in claim 4.

b. The peak current of the anodic pulses is two to three times greater than the peak current of the cathodic pulses, as recited in claim 5.

GB '520 discloses a method for electroplating using bipolar current pulses wherein the anodic pulses have the same or greater value as the peak cathodic current pulses (fig. 1 and 4; page 1, third full paragraph; page 5, second full paragraph). GB '520 teaches that a forward current of 3 amps/Dm and a reverse current of 5 amps/Dm are effective for plating a uniform thickness in holes on a circuit panel (see example results on page 9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method described by Ritzdorf et al., Schumacher et al. and DE '387 to use a higher current (two to three times higher) in the anodic pulses than the cathodic pulses as taught by GB '520 because using a higher anodic current than cathodic current has been shown to deposit a more uniform copper layer in recesses.

Response to Arguments

10. Applicant's arguments filed November 28, 2003, have been fully considered but they are not persuasive.

11. Applicant has presented two main arguments in response to the rejections of the claims. First, Applicant states, "Fe(II) and Fe(III) ions are universally regarded as a semiconductor poison among those of ordinary skill in the semiconductor manufacturing art" (see page 8 of Applicant's response). Second, Applicant states, "[O]ne of ordinary skill in the semiconductor device manufacturing art would never look to a PCB

manufacturing technique to copper plate semiconductor wafers" (see page 8 of Applicant's response).

12. In response to the first argument, no evidence has been provided to support Applicant's allegations that Fe(II) and Fe(III) are "semiconductor poison." Additionally, it is unclear how Applicant's argument applies to the claims as presented. The electrolytic deposition plates copper layers on the basic metal layer. The electrolytic solution never comes into contact with the semiconductor. In this regard, the actual method steps may be used to plate any substrate that has a full-surface basic metal layer coating the substrate.

13. Regarding Applicant's second argument, Landau discloses that electroplating can be equivalently used for plating circuit boards and semiconductor devices. Clearly, one of ordinary skill in the art of semiconductor device manufacturing has looked to PCB manufacturing techniques. As further evidence of the equivalence of semiconductor wafers and printed circuit boards in electrolytic plating methods, U.S. Pat. No. 5,893,966 issued to Akram et al. teach that semiconductor wafers, substrates and printed circuit boards are commonly coated using electrodeposition (see col. 1, lines 15-24). Furthermore, as stated above, the substrate does not appear to limit the actual electrodeposition because the substrate is first coated with a full-surface basic metal layer, which is the only "substrate" that actually contacts the copper deposition bath.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (571) 272-1341. The examiner can normally be reached on Monday-Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

blm
January 14, 2004

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